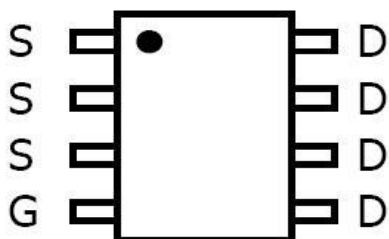
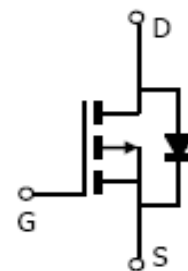


M-MOS Semiconductor Hong Kong Limited
40V P-Channel Enhancement-Mode MOSFET
 $V_{DS} = -40V$
 $R_{DS(ON)}, V_{GS} @ -10V, I_{DS} @ -6.0A = 43m\Omega$
 $R_{DS(ON)}, V_{GS} @ -4.5V, I_{DS} @ -4.0A = 55m\Omega$
Features

Advanced trench process technology

High Density Cell Design For Ultra Low On-Resistance

SO-8

Top View
Internal Schematic Diagram

P-Channel MOSFET
Maximum Ratings and Thermal Characteristics ($T_A = 25^\circ C$ unless otherwise noted)

Parameter	Symbol	Limit	Unit	
Drain-Source Voltage	V_{DS}	-40	V	
Gate-Source Voltage	V_{GS}	± 25		
Continuous Drain Current	I_D	-6	A	
Pulsed Drain Current ¹⁾	I_{DM}	-30		
Maximum Power Dissipation	P_D	$T_A = 25^\circ C$	2.5	W
		$T_A = 75^\circ C$	0.02	
Operating Junction and Storage Temperature Range	T_J, T_{stg}	-55 to 150	$^\circ C$	
Junction-to-Ambient Thermal Resistance (PCB mounted) ²⁾	$R_{\theta JA}$	62.5	$^\circ C/W$	

Note: 1. Repetitive Rating: Pulse width limited by the maximum junction temperature

 2. 1-in² 2oz Cu PCB board

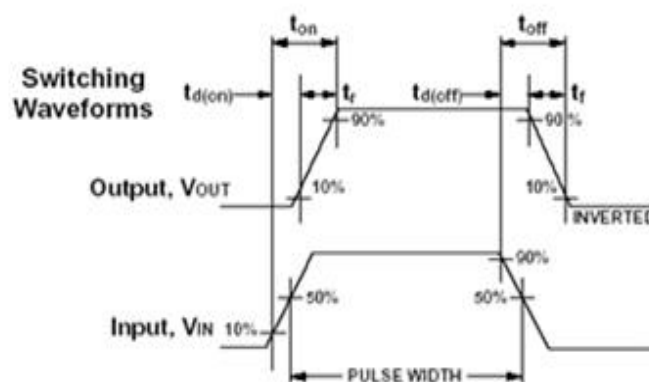
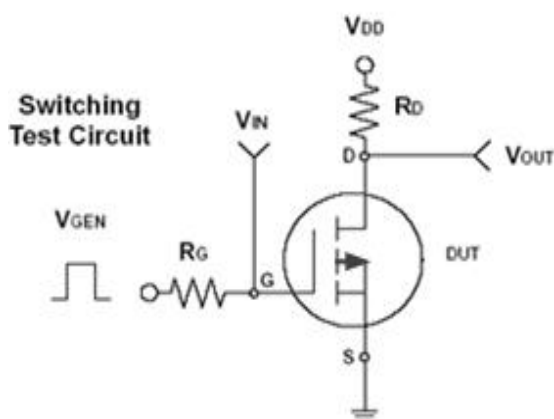
P-Channel Enhancement-Mode MOSFET

ELECTRICAL CHARACTERISTICS

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Static						
Drain-Source Breakdown Voltage	BV_{DSS}	$V_{GS} = 0V, I_D = -250\mu A$	-40			V
Drain-Source On-State Resistance	$R_{DS(on)}$	$V_{GS} = -10V, I_D = -6A$		31.2	43.0	m Ω
Drain-Source On-State Resistance	$R_{DS(on)}$	$V_{GS} = -4.5V, I_D = -4A$		35.9	55.0	
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = -250\mu A$	-1	-1.48	-3	V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = -40V, V_{GS} = 0V$			-1	μA
Gate Body Leakage	I_{GSS}	$V_{GS} = \pm 25V, V_{DS} = 0V$			± 100	nA
Dynamic³⁾						
Total Gate Charge	Q_g	$V_{DS} = -32V, I_D = -6A$ $V_{GS} = -4.5V$		16.00		nC
Gate-Source Charge	Q_{gs}			2.70		
Gate-Drain Charge	Q_{gd}			6.30		
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = -20V, R_L = 20\Omega$ $I_D = -1A, V_{GEN} = -10V$ $R_G = 3.3\Omega$		13.10		ns
Turn-On Rise Time	t_r			5.20		
Turn-Off Delay Time	$t_{d(off)}$			55.70		
Turn-Off Fall Time	t_f			10.70		
Input Capacitance	C_{iss}	$V_{DS} = -25V, V_{GS} = 0V$ $f = 1.0\text{ MHz}$		1272.80		pF
Output Capacitance	C_{oss}			100.50		
Reverse Transfer Capacitance	C_{rss}			83.10		
Source-Drain Diode						
Max. Diode Forward Current	I_S					A
Diode Forward Voltage	V_{SD}	$I_S = -2.0A, V_{GS} = 0V$		0.97	1.2	V

Note: Pulse test: pulse width $\leq 300\mu s$, duty cycle $\leq 2\%$

3. Guaranteed by design; not subject to production testing





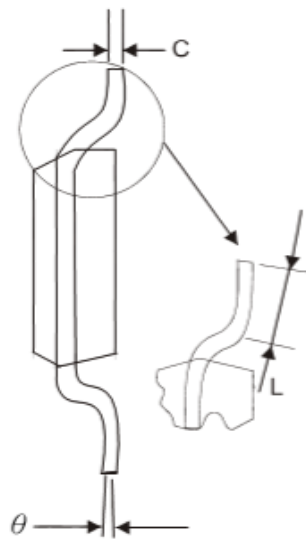
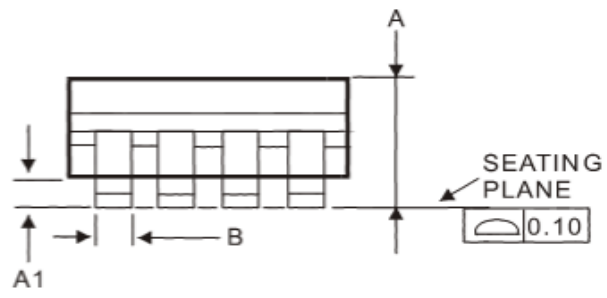
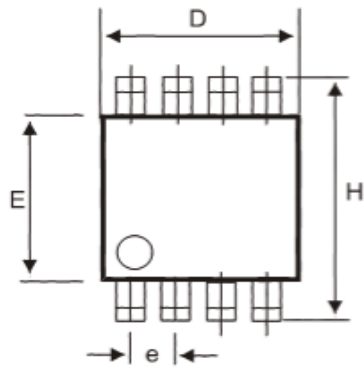
Notice

1. Specification of the products displayed herein are subject to change without notice. Continuous development may necessitate changes in technical data without notice. M-MOS Semiconductor Sdn. Bhd. or anyone on its behalf, assumes no responsibility or liability for any errors or inaccuracies.

2. Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



SOP-8 Package Outline



DIM	MILLIMETERS (mm)	
	MIN	MAX
A	1.35	1.75
A1	0.10	0.25
B	0.35	0.49
C	0.18	0.25
D	4.80	5.00
E	3.80	4.00
e	1.27 BSC	
H	5.80	6.20
L	0.40	1.25
θ	0°	7°